The IEEE Computer Society's Technical Committee on Multiple-Valued Logic will hold its 51st annual symposium in Nursultan, Kazakhstan fully online, on May 25 – 27, 2021. You are invited to submit an original paper, survey, or tutorial paper on any subject in the area of multiple-valued logic, including but not limited to:

- Algebra and Formal Aspects
- Automatic Reasoning
- Logic Programming
- Philosophical Aspects of MVL
- Fuzzy Logic and Soft Computing
- Data Mining
- Machine Learning and Robotics
- Quantum Computing
- Reversible Computing
- Logic Design and Switching Theory
- Test and Verification
- Spectral Techniques
- Circuit/Device Implementation
- VLSI Architecture and Computing
- System-on-Chip Technology
- MVL Aspects of Nanotechnology
- MVL Aspects of Medical Technologies
- MVL Approaches to Big Data

Authors should submit abstract of papers on the conference website by November 1 – December 21, 2020 (extended!), and then, submit papers in PDF format by November 8 – December 28, 2020. Each manuscript should include a 50-to-100 word abstract, and should not exceed 6 pages in the 2-column IEEE Proceedings format. The proceedings of ISMVL are in the Ei compendex that is the broadest and most complete engineering literature database available in the world. Special issues of some journals are planned for selected ISMVL 2021 papers.

Authors will be notified about acceptance by February 1 – March 1, 2021. Camera-ready copies of accepted papers are due on March 1 – April 1, 2021. For submission details, please visit the symposium website:

http://mvl.jpn.org/ISMVL2021/

The symposium will be co-located with the 30th International Workshop on Post-Binary ULSI Systems and Reed-Muller 2021 Workshop. Information on accommodations and transportation to the Nursultan will be provided at a later date. This event is sponsored by the IEEE Computer Society. For additional information, please contact:

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